



Welcome United States Patent and Trademark Office

Search Results

EROSSE

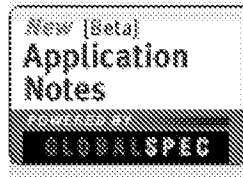
SEARCH

SEE AFLORE GUIDE

Results for "((pipeline)<in>metadata) <and> ((bank)<in>metadata) <and> ((performance..."

Your search matched 36 of 1776775 documents.

A maximum of 36 results are displayed, 25 to a page, sorted by Relevance in Descending order.



- Search Options

[View Session History](#)

[New Search](#)

✓ Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

Moody Season

(((pipeline)<in>metadata) <and> ((bank)<in>metadata))<and> ((performance)<in>

///

☐ Check to search only within this results set

Display Format:



Citation



Citation & Abstract

IEEE/ET

Books

Educational Courses

IEEE/ET journals, transactions, letters, magazines, conference proceedings, and standards.

view selected items

Select All Deselect All



1. Scalar memory references in pipelined multiprocessors: a performance study
Ganesan, R.; Weiss, S.;
[Software Engineering, IEEE Transactions on](#)
Volume 18, Issue 1, Jan. 1992 Page(s):78 - 86
Digital Object Identifier 10.1109/32.120318

AbstractPlus | Full Text: PDF(712 KB) IEEE JNL
Rights and Permissions



2. A 75-mW, 10-b, 20-MSPS CMOS subranging ADC with 9.5 effective bits at Nyquist
Brandt, B.P.; Lutsky, J.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 34, [issue 12](#), Dec. 1999 Page(s):1788 - 1795
Digital Object Identifier 10.1109/4.808903

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(444 KB\)](#) | [IEEE JNL](#)
[Rights and Permissions](#)



3. Implementation of a Parallel and Pipelined Watershed Algorithm on FPGA
Dang Ba Khac Trieu; Tsutomu Maruyama;
[Field Programmable Logic and Applications, 2006. FPL '06. International Conference on](#)
Aug. 2006 Page(s):1 - 6
Digital Object Identifier 10.1109/FPL.2006.311267

[AbstractPlus](#) | [Full Text: PDF\(300 KB\)](#) | [ISSN: 0959-2688](#)
[Rights and Permissions](#)



4. Block, multistride vector, and FFT accesses in parallel memory systems
Harper, D.T., III;
[Parallel and Distributed Systems, IEEE Transactions on](#)
Volume 2, Issue 1, Jan. 1991 Page(s):43 - 51
Digital Object Identifier 10.1109/71.80188








[AbstractPlus](#) | [Full Text: PDF \(836 KB\)](#) | [HTML](#)
[Rights and Permissions](#)



5. Models of access delays in multiprocessor memories
Bucher, I.Y.; Calahan, D.A.;
Parallel and Distributed Systems, IEEE Transactions on
Volume 3, Issue 3, May 1992 Page(s):270 - 280
Digital Object Identifier 10.1109/71.139201

[AbstractPlus](#) | [Full Text: PDF\(912 KB\)](#) [IEEE JNL](#)
[Rights and Permissions](#)

6. Power-aware branch prediction: characterization and design

-  Parikh, D.; Skadron, K.; Zhang, Y.; Stan, M.;
Computers, IEEE Transactions on
Volume 53, Issue 2, Feb 2004 Page(s):168 - 186
Digital Object Identifier 10.1109/TC.2004.1261827
[AbstractPlus](#) | Full Text: [PDF\(7587 KB\)](#) | [IEEE JNL](#)
[Rights and Permissions](#)
-  7. Scalar operand networks
Taylor, M.D.; Lee, W.; Amarasinghe, S.P.; Agarwal, A.;
Parallel and Distributed Systems, IEEE Transactions on
Volume 16, Issue 2, Feb 2005 Page(s):145 - 162
Digital Object Identifier 10.1109/TPDS.2005.24
[AbstractPlus](#) | Full Text: [PDF\(1864 KB\)](#) | [IEEE JNL](#)
[Rights and Permissions](#)
-  8. Design and evaluation of a network-based architecture for cryptographic devices
Dilparic, L.; Arvind, D.K.;
Application-Specific Systems, Architectures and Processors, 2004. Proceedings. 15th IEEE International Conference on
2004 Page(s):191 - 201
Digital Object Identifier 10.1109/ASAP.2004.1342470
[AbstractPlus](#) | Full Text: [PDF\(377 KB\)](#) | [IEEE CONF](#)
[Rights and Permissions](#)
-  9. Asynchronous DRAM design and synthesis
Ekanayake, V.N.; Manohar, R.;
Asynchronous Circuits and Systems, 2003. Proceedings. Ninth International Symposium on
12-15 May 2003 Page(s):174 - 183
Digital Object Identifier 10.1109/ASYNC.2003.1199177
[AbstractPlus](#) | Full Text: [PDF\(469 KB\)](#) | [IEEE CONF](#)
[Rights and Permissions](#)
-  10. An interprocessor memory access arbitrating scheme for the S-3800 vector supercomputer
Sakakibara, T.; Kitai, K.; Isobe, T.; Yazawa, S.; Tanaka, T.; Tamaki, Y.; Inagami, Y.;
Parallel Architectures, Algorithms and Networks, 1994. (ISPAN) International Symposium on
14-16 Dec. 1994 Page(s):262 - 269
Digital Object Identifier 10.1109/ISPAN.1994.367140
[AbstractPlus](#) | Full Text: [PDF\(456 KB\)](#) | [IEEE CONF](#)
[Rights and Permissions](#)
-  11. Architecture synthesis of high-performance application-specific processors
Breternitz, M., Jr.; Shen, J.P.;
Design Automation Conference, 1990. Proceedings. 27th ACM/IEEE
24-28 June 1990 Page(s):542 - 548
Digital Object Identifier 10.1109/DAC.1990.114915
[AbstractPlus](#) | Full Text: [PDF\(668 KB\)](#) | [IEEE CONF](#)
[Rights and Permissions](#)
-  12. On-Chip Adaptive Circuits for Fast Media Processing
Sangireddy, R.; Somani, A.K.;
Circuits and Systems II: Express Briefs, IEEE Transactions on [see also Circuits and Systems II: Analog and Digital Integrated Circuits and Systems, IEEE Transactions on]
Volume 53, Issue 3, Sept. 2006 Page(s):946 - 950
Digital Object Identifier 10.1109/TCSII.2006.880336
[AbstractPlus](#) | Full Text: [PDF\(640 KB\)](#) | [IEEE JNL](#)
[Rights and Permissions](#)
-  13. The Organization and Use of Parallel Memories
Budnik, P.; Kuck, D.J.;
Computers, IEEE Transactions on
Volume C-20, Issue 12, Dec. 1971 Page(s):1566 - 1569
[AbstractPlus](#) | Full Text: [PDF\(816 KB\)](#) | [IEEE JNL](#)
[Rights and Permissions](#)
-  14. A Pipeline Implementation of a Watershed Algorithm on FPGA
Dang Ba Khac Trieu; Maruyama, T.;
Field Programmable Logic and Applications, 2007. FPL 2007. International Conference on
27-29 Aug. 2007 Page(s):714 - 717

Digital Object Identifier 10.1109/FPL.2007.4380752

[AbstractPlus](#) | Full Text: [PDF\(387 KB\)](#) | [IEEE CNF](#)

[Rights and Permissions](#)



15. Classification of Infrasound Surf Events Using Parallel Neural Network Banks
Ham, F.M.; Acharyya, R.; Lee, Y.-C.; Garcés, M.; Fee, D.; Whitten, C.; Rivera, E.;
[Neural Networks, 2007. IJCNN 2007. International Joint Conference on](#)
12-17 Aug. 2007 Page(s):720 - 725
Digital Object Identifier 10.1109/IJCNN.2007.4371046

[AbstractPlus](#) | Full Text: [PDF\(359 KB\)](#) | [IEEE CNF](#)

[Rights and Permissions](#)



16. Design of a Field-Programmable Dual-Precision Floating-Point Arithmetic Unit
Diniz, P.C.; Govindu, G.;
[Field Programmable Logic and Applications, 2006. FPL '06. International Conference on](#)
Aug. 2006 Page(s):1 - 4
Digital Object Identifier 10.1109/FPL.2006.311302

[AbstractPlus](#) | Full Text: [PDF\(428 KB\)](#) | [IEEE CNF](#)

[Rights and Permissions](#)



17. A study of the on-chip interconnection network for the IBM Cyclops64 multi-core architecture
Ying Ping Zhang; Taikyeong Jeong; Fei Chen; Haiping Wu; Nitzsche, R.; Gao, G.R.;
[Parallel and Distributed Processing Symposium, 2006. IPDPS 2006. 20th International](#)
25-29 April 2006 Page(s):10 pp.
Digital Object Identifier 10.1109/IPDPS.2006.1639301

[AbstractPlus](#) | Full Text: [PDF\(184 KB\)](#) | [IEEE CNF](#)

[Rights and Permissions](#)



18. High-performance longest prefix matching supporting high-speed incremental updates and guarant
Sundström, M.; Larzon, L.-A.;
[INFOCOM 2005. 24th Annual Joint Conference of the IEEE Computer and Communications Societies. Proc](#)
Volume 3, 13-17 March 2005 Page(s):1641 - 1652 vol. 3
Digital Object Identifier 10.1109/INFOCOM.2005.1498446

[AbstractPlus](#) | Full Text: [PDF\(797 KB\)](#) | [IEEE CNF](#)

[Rights and Permissions](#)



19. Pipelined orthogonal subband affine projection filters and its efficient implementation
Hun Choi; Jo-Dong Park; Sang-Wook Sohn; Hyeon-Deok Bae;
[Digital Signal Processing Workshop, 2004 and the 3rd IEEE Signal Processing Education Workshop, 2004.](#)
1-4 Aug. 2004 Page(s):102 - 106
Digital Object Identifier 10.1109/DSPWS.2004.1437920

[AbstractPlus](#) | Full Text: [PDF\(325 KB\)](#) | [IEEE CNF](#)

[Rights and Permissions](#)



20. Non-uniform access asynchronous register files
Fang, D.; Manohar, A.;
[Asynchronous Circuits and Systems, 2004. Proceedings. 15th International Symposium on](#)
19-23 April 2004 Page(s):78 - 85
Digital Object Identifier 10.1109/ASYNC.2004.1299289

[AbstractPlus](#) | Full Text: [PDF\(1497 KB\)](#) | [IEEE CNF](#)

[Rights and Permissions](#)



21. Efficient IMDCT core designs for audio signal processing
Po-sheng Wu; Yin-Tsung Hwan;
[Signal Processing Systems, 2003. SIPS 2003. IEEE Workshop on](#)
27-29 Aug. 2003 Page(s):275 - 280

[AbstractPlus](#) | Full Text: [PDF\(437 KB\)](#) | [IEEE CNF](#)

[Rights and Permissions](#)



22. Scalar operand networks: on-chip interconnect for ILP in partitioned architectures
Bedford Taylor, M.; Lee, W.; Amarasinghe, S.; Agarwal, A.;
[High-Performance Computer Architecture, 2003. HPCA-9 2003. Proceedings. The Ninth International Symp](#)
8-12 Feb. 2003 Page(s):341 - 353
Digital Object Identifier 10.1109/HPCA.2003.1183551

[AbstractPlus](#) | Full Text: [PDF\(10255 KB\)](#) | [IEEE CNF](#)

[Rights and Permissions](#)



23. Optimizing loop performance for clustered VLIW architectures

Yi Qian; Carr, S.; Sweany, P.;

Parallel Architectures and Compilation Techniques, 2002. Proceedings. 2002 International Conference on
22-25 Sept. 2002 Page(s):271 - 280

Digital Object Identifier 10.1109/PACT.2002.1106026

[AbstractPlus](#) | Full Text: [PDF\(282 KB\)](#) [IEEE CDF](#)[Rights and Permissions](#)

24. Efficient VLSI architectures for the biorthogonal wavelet transform by filter bank and lifting scheme

Jer Min Jou; Yeu-Hong Shiau; Chin-Chi Liu;

Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on
Volume 2, 6-9 May 2001 Page(s):529 - 532 vol. 2

Digital Object Identifier 10.1109/ISCAS.2001.921124

[AbstractPlus](#) | Full Text: [PDF\(344 KB\)](#) [IEEE CDF](#)[Rights and Permissions](#)

25. Multiple-banked register file architectures

Cruz, J.-L.; Gonzalez, A.; Valero, M.; Topham, N.P.;

Computer Architecture, 2000. Proceedings of the 27th International Symposium on
2000 Page(s):316 - 325

[AbstractPlus](#) | Full Text: [PDF\(800 KB\)](#) [IEEE CDF](#)[Rights and Permissions](#)[Help](#) [Cor](#)

Indexed by

